



## TSMC and ANSYS Accelerate Automotive Reliability Solutions

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PITTSBURGH, Oct. 3, 2018 /PRNewswire/ -- Customers of [TSMC](#) and [ANSYS](#) (NASDAQ: ANSS) can accelerate the production of automotive design features through the Automotive Reliability Solution Guide 2.0, an outline of proven workflows to support customers' intellectual property (IP), chip and package development for TSMC 7nm FinFET(N7) process technology. Based on TSMC and ANSYS collaboration on reliability solutions in ANSYS® RedHawk™, ANSYS® RedHawk-CTA™, ANSYS® Totem™ and ANSYS® Pathfinder-Static™, the expanded guide empowers customers to develop more efficient and robust chips for the next generation of smart automobiles.

image

Reliability is critical for the cutting-edge automotive platforms used in advanced driver assistance systems, infotainment controls and autonomous driving. The expanded guidelines incorporate various reliability capabilities in one place to support mutual customers' IP, chip and package development for automotive applications in TSMC's N7 process technology. The guide includes workflows for electromigration (EM), thermal reliability including self-heat and chip package thermal co-analysis and electrostatic discharge. It also includes a new workflow for statistical electromigration budgeting (SEB).

SEB enables chip designers to meet stringent safety and reliability requirements by prioritizing the most important EM fixes for signoff while avoiding over design to achieve lower cost, higher performance and greater product reliability. RedHawk and Totem are enabled with advanced SEB modeling for TSMC's latest FinFET process technology.

"The IPs and Systems-on-Chips (SoCs) designed for automotive applications using TSMC's N7 process technology offer increased integration, functionality and operating speeds but must meet rigorous requirements for functional safety and reliability," said Suk Lee, Senior Director, Design Infrastructure Marketing Division at TSMC. "The Automotive Reliability Solution Guide 2.0 helps customers to meet reliability goals and deliver products to the market faster with greater confidence."

"Safety and reliability standards are increasingly stringent in next-generation automotive systems, mandating the need for a comprehensive multi-physics simulation platform that simultaneously solves for thermal effects, reliability, power-timing and performance across the spectrum of chip, package and system," said John Lee, General Manager at ANSYS. "Reliability workflows presented in the Automotive Reliability Solution Guide 2.0 empower mutual customers to accelerate the development of IPs, SoCs and packages that meet elevated reliability and safety requirements, while avoiding over design."

Workflows within the Automotive Reliability Guide 2.0 are based on the following ANSYS products:

- **ANSYS RedHawk:** The industry's go-to power integrity and reliability sign-off solution for SoCs. With a track record of thousands of designs in silicon, RedHawk enables users to create high-performance SoCs that are still power efficient and reliable against thermal, EM and electrostatic discharge (ESD) issues for markets such as mobile, communications, high-performance computing, automotive and IoT.
- **ANSYS RedHawk-CTA:** An integrated chip–package co-analysis and co-visualization solution, RedHawk-CTA enables engineers to accurately model the thermal behavior of the chip and package by solving the power/thermal convergence loop. It also creates a proprietary chip thermal model that captures the power and current inside a chip as a function of temperature and layer-wise metal density for accurate system level simulation.
- **ANSYS Totem:** Transistor level power integrity and reliability signoff solution for full-custom/analog and mixed-signal designs. In addition to static IR and dynamic voltage drop analysis, Totem can include the substrate network, along with package and board models, for chip-package-system co-analysis. Totem can also perform thermal-aware power and signal line electromigration analyses for analog, mixed-signal designs.
- **ANSYS PathFinder:** ANSYS PathFinder helps users plan, verify and sign-off IP and full-chip SoC designs for integrity and robustness against ESD. The analysis is performed at the layout and circuit levels to help user identify and isolate design issues that can cause chip or IP failure from charged-device model, human body model or other ESD events.

Customers may request the Automotive Reliability Guide 2.0 [here](#).

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