



ANSYS And Synopsys To Partner In Accelerating Robust Design Optimization For Next Generation High-Performance Computing, Mobile And Automotive Products

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PITTSBURGH and MOUNTAIN VIEW, Calif., June 19, 2017 /PRNewswire/ -- [ANSYS](#) (NASDAQ: ANSS) and [Synopsys](#) (NASDAQ: SNPS) will enable customers to accelerate the next generation of high-performance computing, mobile and automotive products thanks to a new partnership that will tightly integrate ANSYS' power integrity and reliability signoff technologies with Synopsys' physical implementation solution for in-design usage.

image

Developers of innovative, cost-effective and reliable smart products need to quickly optimize, validate and signoff their designs. While designers have been using ANSYS and Synopsys tools in combination for years, the integrated solution will enable mutual customers to apply power integrity and reliability signoff technologies earlier in the design flow – empowering them to deliver innovative, high-performance and reliable products faster, while reducing power, area and cost.

The integration of ANSYS' industry-leading platform for chip power and reliability signoff, ANSYS® RedHawk™, with Synopsys' best-in-class place-and-route solutions, Synopsys IC Compiler™ II, will provide users earlier signoff accuracy within the Synopsys design environment. This integration will enable rapid design exploration, design weakness detection, optimization and thermal-aware reliability through increased functionality within the place-and-route environment. The in-design power integrity and reliability signoff-driven flow will eliminate late design changes and ensure consistency with final chip-package-system signoff analyses with RedHawk.

"This partnership is a continued step in Synopsys' strategy to bring more physical and signoff technologies earlier in the design flow within our Synopsys Digital Design Platform," said Sassine Ghazi, senior vice president and co-general manager, Design Group at Synopsys. "Partnering with ANSYS enables Synopsys to quickly deliver a reliability and thermal-driven design flow that is critical for designing the next generation of semiconductors."

Synopsys and ANSYS will also provide a feedback loop between the two-gold standard solutions, Synopsys PrimeTime® and ANSYS RedHawk. Voltage-aware timing analysis can be performed rapidly to avoid additional guard-banding and design margining.

"As the industry moves to more and more complex chips, signoff-driven rail analysis needs to be available sooner in the physical design flow just like timing and design rule checking," said John Lee, general manager at ANSYS. "We believe partnering with Synopsys to bring our signoff technology into the Synopsys In-Design approach is the right way to accomplish this objective."

"TSMC collaborates with our EDA partners on silicon design solutions to enable our customers to achieve competitive performance, power and area for their next generation electronic products," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "This industry collaboration between Synopsys and ANSYS provides an opportunity for them to take the collaboration a step further by enabling reliability and thermal-driven physical design built on the industry's popular physical implementation and signoff solutions."

"ARM has been a long-time user of both Synopsys and ANSYS technologies, which have helped in the development of some of the most sophisticated CPU cores available in the market," said Hobson Bullman, vice president and general manager, TSG, ARM. "This announced partnership will enable our semiconductor partners to optimize our IP within their SoC designs earlier in the flow allowing more time to focus on reliable, robust and energy efficient designs."

"Both Synopsys and ANSYS have been strong collaboration partners with MediaTek to manage increasing manufacturing complexity and to deliver designs on schedule while realizing aggressive performance, power and area goals," said SA Hwang, general manager of Design Technology, MediaTek. "We believe this new partnership between Synopsys and ANSYS will enable MediaTek engineers to accelerate their pace of innovation while achieving further power, performance and area optimizations."

ANSYS and Synopsys will be featured at the Design Automation Conference in booth 647 and booth 147 respectively, from June 18-22 in Austin, Texas.

About ANSYS, Inc.

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About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-

on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the intended integration of ANSYS' technology with Synopsys' platform and the expected benefits of such arrangement and integration. Forward-looking statements are subject to both known and unknown risks and uncertainties that may cause actual results to differ materially from those expressed or implied in the forward-looking statements. Such risks and uncertainties include, among others, the ability of the parties to finalize the details of the planned agreement, Synopsys' ability to integrate ANSYS' technology with its own successfully, and the companies' abilities to market the solution. Other risks and uncertainties that may apply are set forth in the Risk Factors section of each company's most recently filed Quarterly Report on Form 10-Q. Neither party assume any obligation to update any forward-looking statement contained in this press release.

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