Apache Design Releases Fourth-Generation RedHawk for Sub-20 Nanometer Power Sign-off

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PITTSBURGH, May 1, 2012 /PRNewswire/ -- ANSYS (NASDAQ: ANSS) subsidiary Apache Design, Inc. today introduced RedHawk™-3DX to meet the power, performance and price demands of low-power mobile, high-performance computing, consumer and automotive electronics. This fourth-generation power sign-off solution delivers greater accuracy, capacity and usability for full-chip dynamic power and reliability simulation to manage power consumption and improve power delivery efficiency of advanced integrated circuit (IC) designs.

(Logo: http://photos.prnewswire.com/prnh/20110127/MM38081LOGO)

The release of RedHawk-3DX extends previous generations' capabilities to address sub-20 nanometer (nm) designs with 3+ gigahertz performance and billions of gates. It is also architected to support the simulation of emerging chip and packaging technologies using multidie three-dimensional ICs (3D-ICs) for smart electronic products.

"For more than a decade, RedHawk has been the industry standard for solving critical power integrity issues and is used as a sign-off solution by most of the world's top 20 semiconductor companies," said Dr. Andrew Yang, president of Apache Design, Inc., and vice president and general manager of ANSYS. "As power, performance and price drive advancements in semiconductors, our customers need best-in-class solutions to stay competitive. The release of RedHawk-3DX demonstrates our strong commitment in continuing to deliver innovative technologies to meet our customers' next-generation low-power requirements and capacity challenges."

Sign-off Accuracy and Coverage

To ensure the performance of next-generation ICs, engineers need greater power simulation accuracy and a more comprehensive understanding of power behavior scenarios. RedHawk-3DX improves the accuracy and coverage of dynamic power analysis by providing enhanced logic-handling capabilities. Its new event- and state-propagation technologies with vector-based and VectorLess™ modes utilize both the functional stimulus and statistical probability to determine the switching scenario of the design. The fast event-propagation engine uses register transfer language (RTL)-level functional stimulus to perform cycle-accurate voltage drop simulation. The robust state-propagation engine for the VectorLess mode enables time-domain transient analysis without actual input stimulus and includes proprietary techniques to eliminate underestimation of toggle rates associated with traditional activity-based propagation approaches. RedHawk-3DX also supports flexible mixed-excitation mode, in which some blocks use RTL or gate-level vectors while the rest of the design uses the VectorLess methodology.

Sub-20 nm design requirements for power and signal electromigration (EM) analyses are driving the need for a more accurate reliability sign-off solution. RedHawk-3DX advances EM modeling technologies by delivering current direction-aware, metal topology-aware and temperature-aware EM checks, and by expanding its capabilities to support leading foundries' complex 20 nm EM rules.

Improved Capacity and Performance
To meet next-generation system-on-chip (SoC) and multidie simulation capacity challenges, RedHawk-3DX provides a hierarchical extraction methodology and a re-architected transient simulation engine, delivering up to 40 percent speed improvement without sacrificing sign-off accuracy. The new extraction reuse view (ERV) technology optimizes a majority of the design while allowing selected critical blocks to retain full-layout details, enabling full-chip simulation with complete consideration for package impact. This approach is particularly effective in handling multicore designs. Additional performance improvements are enabled through a redesigned simulation kernel, which uses advanced multithreaded software architecture.

Support of Advanced Low-Power Techniques

Advanced low power designs face increasing power/ground noise across the IC, package and system, which can significantly impact overall performance and silicon success. So it is critical to maintain the voltage quality on the ICs. Designers use on-chip low-drop-out (LDO) voltage regulators to ensure that the output voltage is maintained throughout various operating conditions. RedHawk-3DX enables the creation of an accurate LDO behavioral model for full-chip static and dynamic simulations to help detect and predict excessive load and line regulations.

Multidie/3D-IC Extension
Emerging chip and packaging technologies for stacked-die, 3D-IC architecture help to reduce IC power consumption. RedHawk-3DX provides a 3D-IC extension to support both concurrent and model-based multidie simulations of designs with silicon interposer and through-silicon vias (TSVs). The concurrent mode enables simulation of all chips including the interposer in full layout detail, whereas a model-based approach allows the use of a Chip Power Model (CPM™) for some of the chips.

RedHawk-3DX introduces a new multitab, multipane graphical user interface that enables greater flexibility and productivity for analyzing multidie designs. It provides the ability to view voltage drop hotspots and other results from multiple chips in a 3-D stack-up simultaneously. This versatile user environment, in conjunction with Apache's RedHawk Explorer, enables designers to qualify input data, review overall design weaknesses and debug specific hotspots – providing feedback that can lead to more robust designs.

For related downloadable images, visit www.ansys.com/newsimages.

About RedHawk
RedHawk allows designers to explore and identify physical design weaknesses that can result in power delivery failure, automatically repair the supply noise source, analyze the impact of dynamic voltage drop on timing and jitter, verify power and signal electromigration (EM), validate robustness of electrostatic discharge (ESD) protection circuitry using PathFinder™, and provide a power delivery network (PDN) model for system-level analysis using the Chip Power Model. RedHawk-3DX also leverages Apache's RTL Power Model (RPM™) to provide more realistic switching activities for

accurate power sign-off.

About Apache Design, Inc.

Apache Design, an ANSYS subsidiary, enables simulation-driven IC and electronic systems design by providing advanced chip-level power analysis, optimization, and sign-off solutions. Apache's integrated products and methodologies advance low-power innovation and address chip-package-system power and noise challenges. Using Apache's engineering simulation software early in the design and throughout the process enables the world's top semiconductor companies to gain a competitive advantage delivering more power-efficient, high-performance, and noise immune chips. Apache's products help lower power consumption, increase operating performance, mitigate design risks, reduce system cost, and shorten time-to-market for a broad range of end-markets and applications. Learn more at: http://www.apache-da.com/.

About ANSYS, Inc.

ANSYS brings clarity and insight to customers' most complex design challenges through fast, accurate and reliable engineering simulation. Our technology enables organizations — no matter their industry — to predict with confidence that their products will thrive in the real world. Customers trust our software to help ensure product integrity and drive business success through innovation. Founded in 1970, ANSYS employs more than 2,200 professionals, many of them expert in engineering fields such as finite element analysis, computational fluid dynamics, electronics and electromagnetics, and design optimization. Headquartered south of Pittsburgh, U.S.A., ANSYS has more than 60 strategic sales locations throughout the world with a network of channel partners in 40+ countries. Visit www.ansys.com for more information.

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